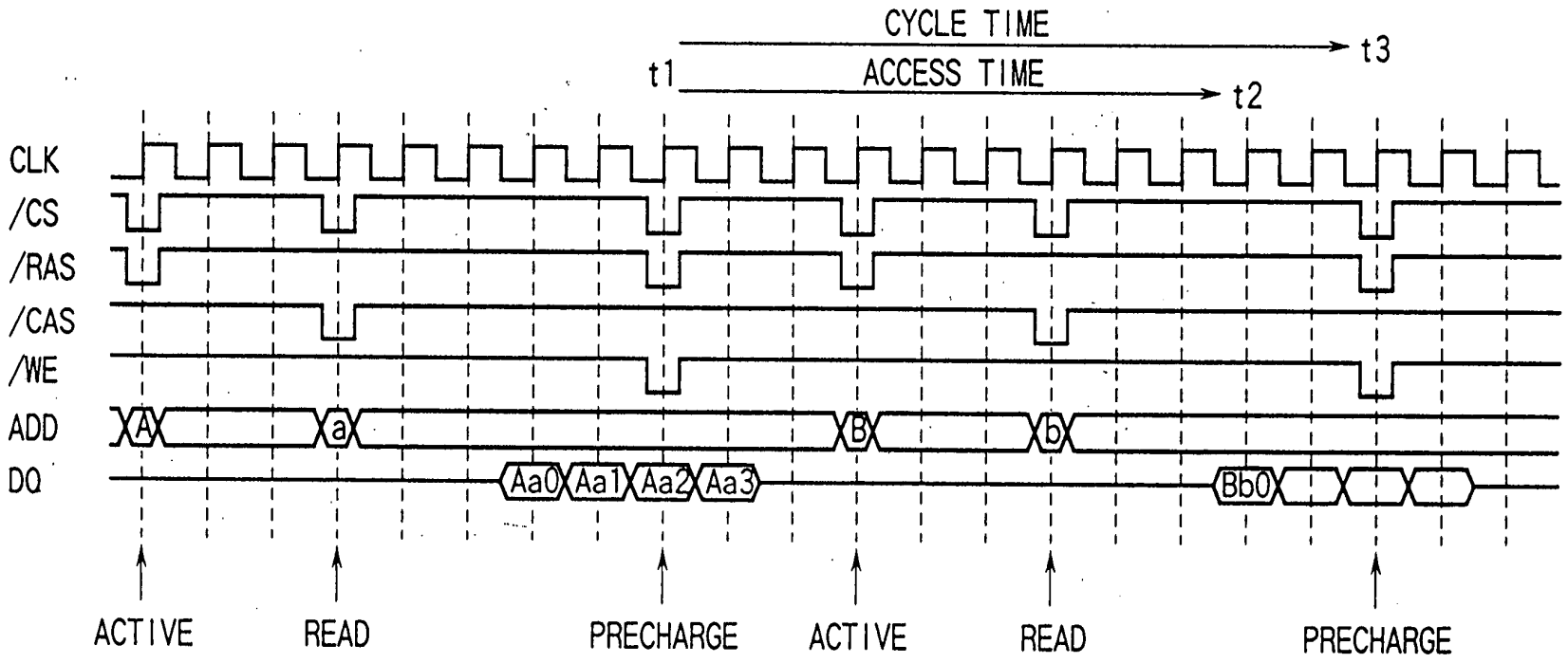

FIG. 1 PRIOR ART

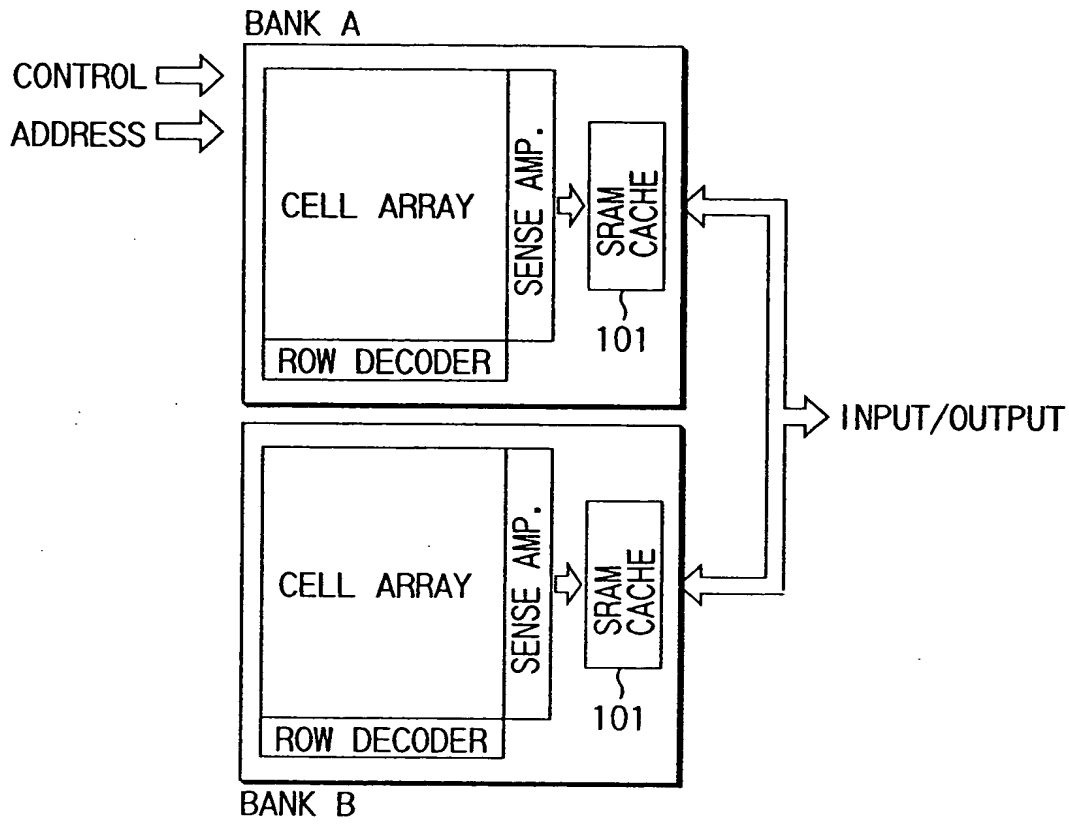

FIG. 2 PRIOR ART

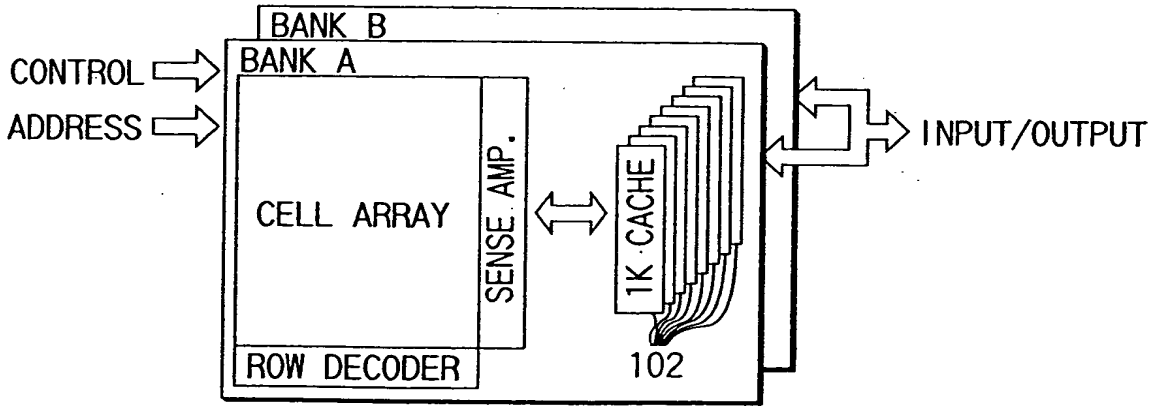

FIG. 3 PRIOR ART

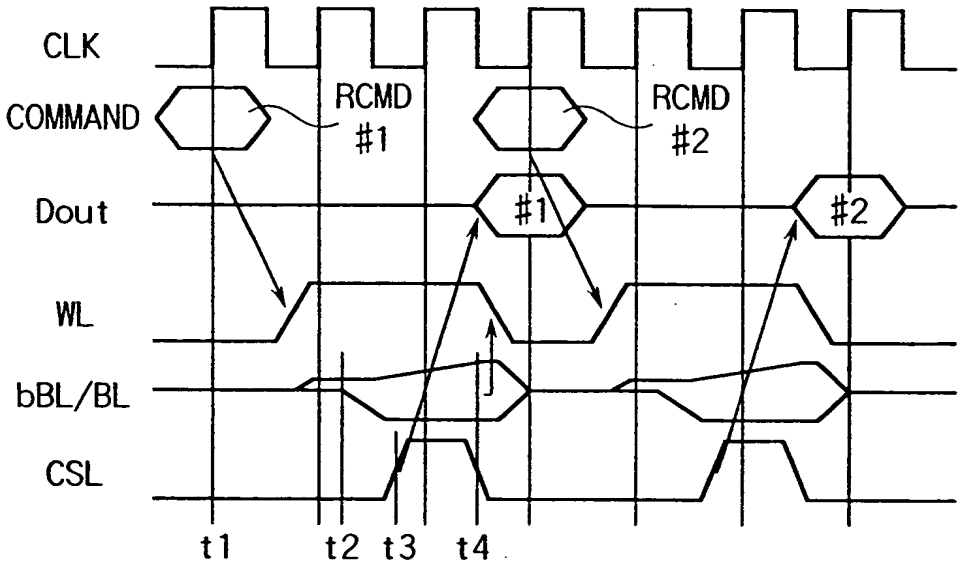

FIG. 4
PRIOR ART

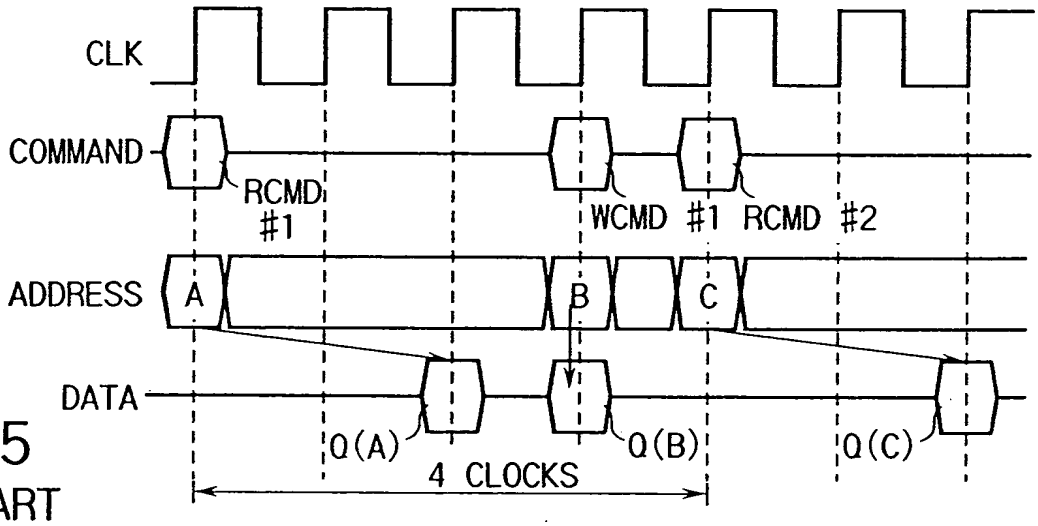

FIG. 5
PRIOR ART

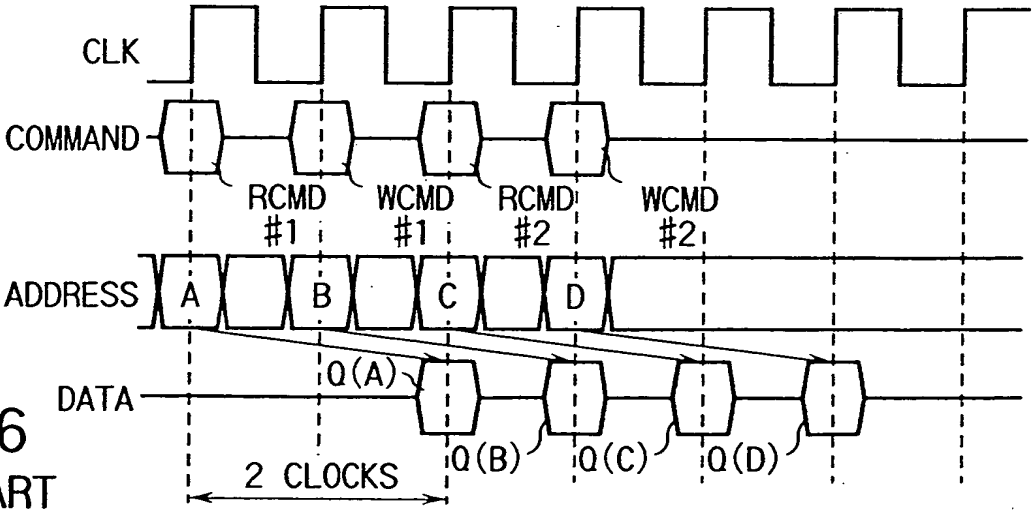

FIG. 6
PRIOR ART

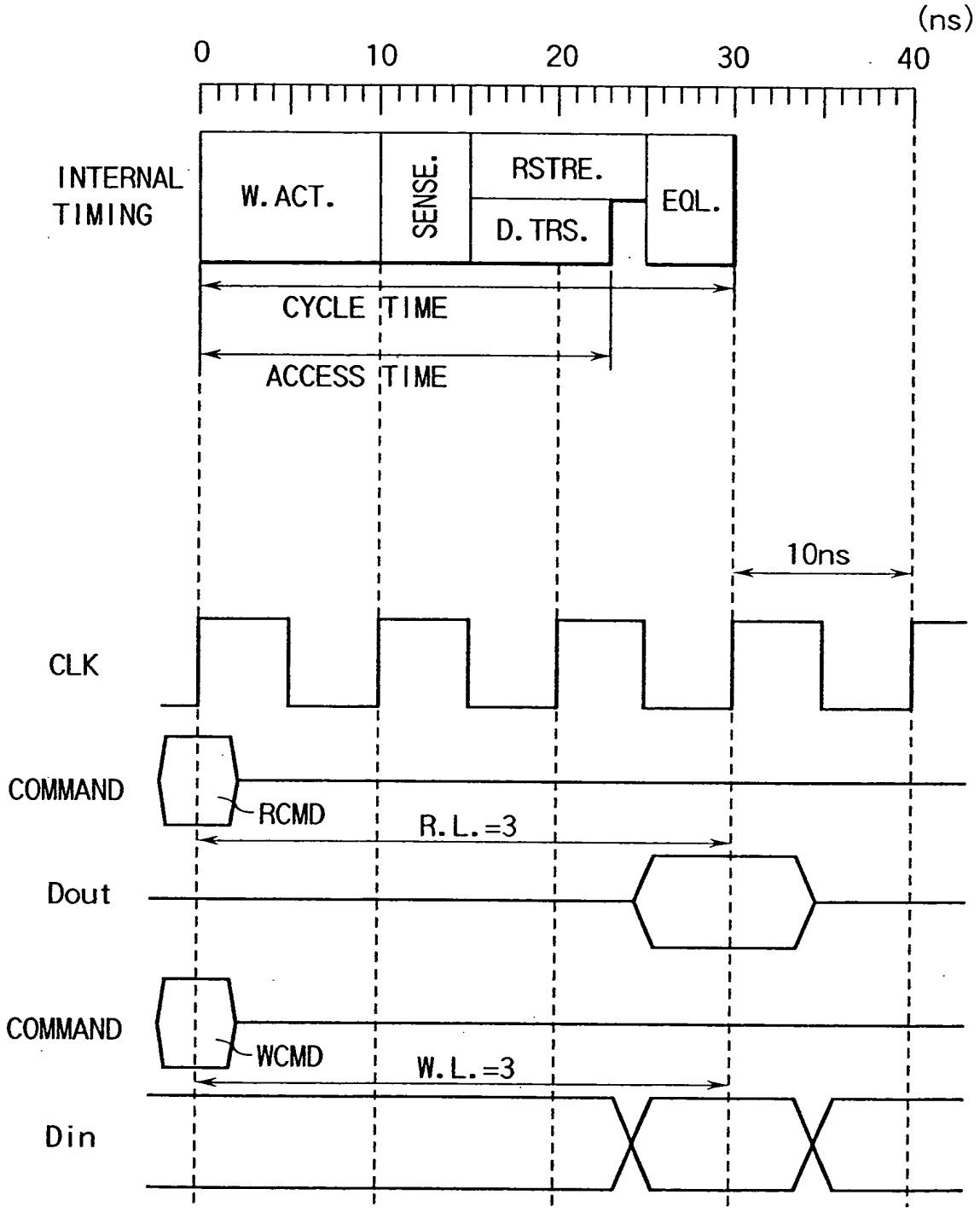

FIG. 7 PRIOR ART

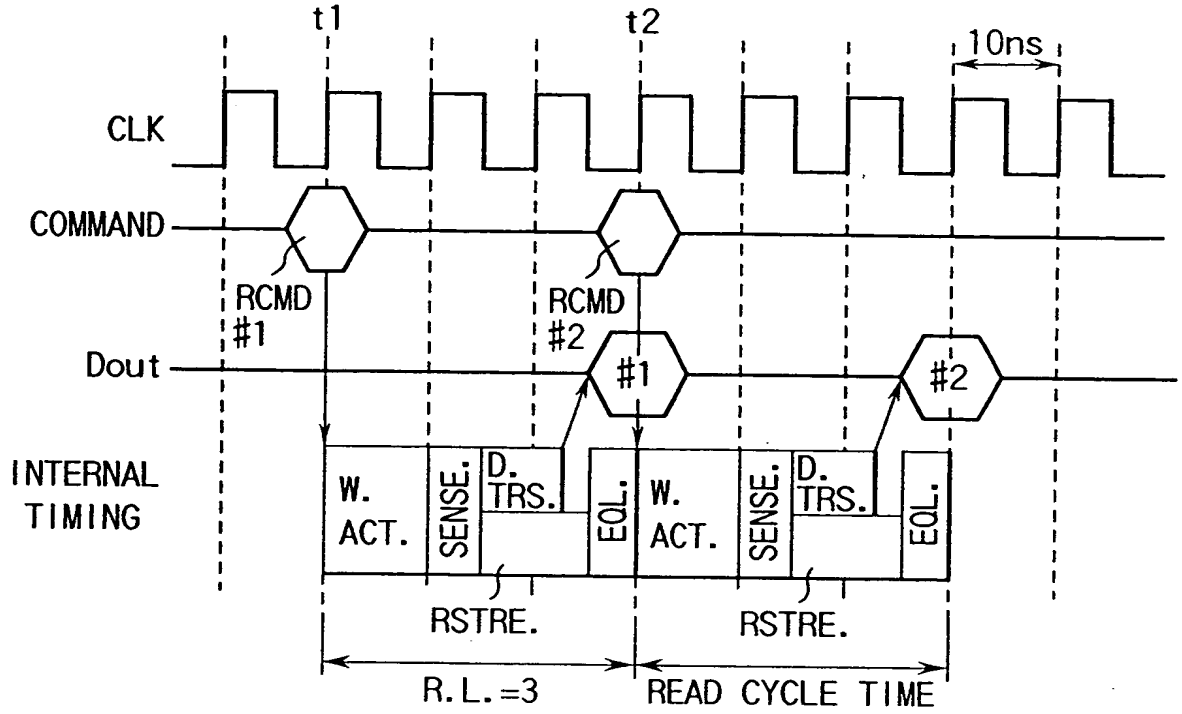
t1
t2
10ns
CLK
COMMAND
RCMD #1
RCMD #2
Dout
#1
#2
INTERNAL TIMING
W. ACT.
SENSE.
D. TRS.
EQL.
W. ACT.
SENSE.
D. TRS.
EQL.
RSTRE.
RSTRE.
R.L.=3
READ CYCLE TIME

FIG. 8A

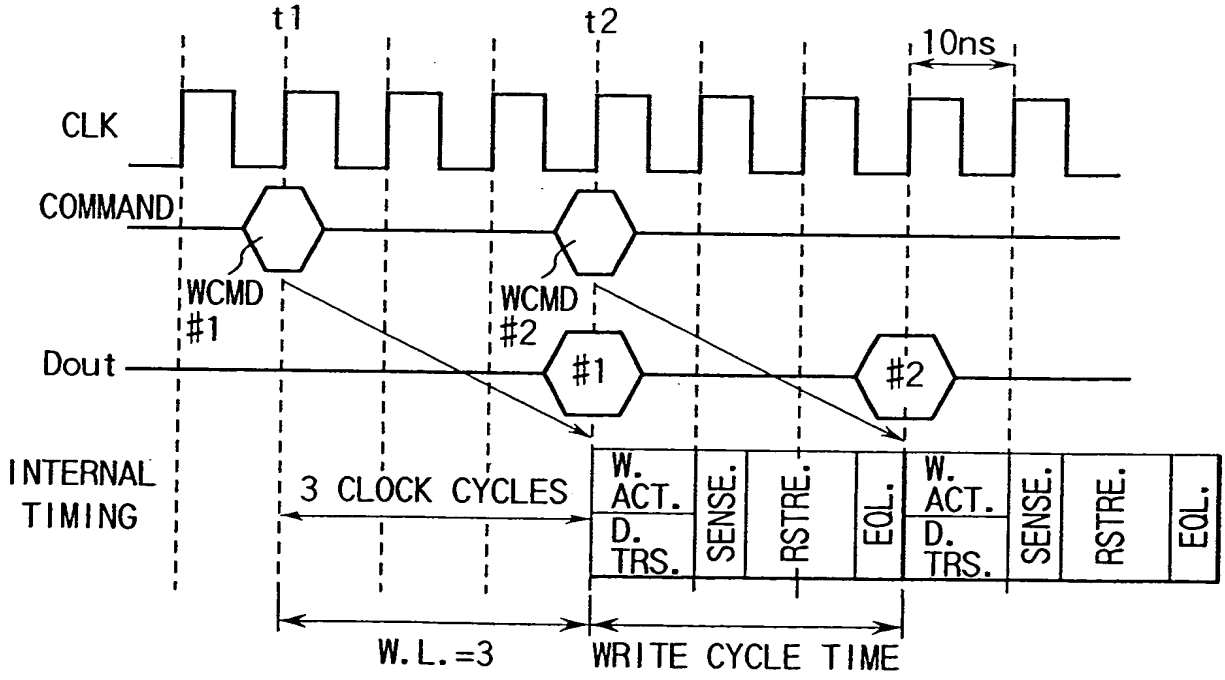
t1
t2
10ns
CLK
COMMAND
WCMD #1
WCMD #2
Dout
#1
#2
INTERNAL TIMING
3 CLOCK CYCLES
W. ACT.
D. TRS.
SENSE.
RSTRE.
EQL.
W. ACT.
D. TRS.
SENSE.
RSTRE.
EQL.
W.L.=3
WRITE CYCLE TIME

FIG. 8B

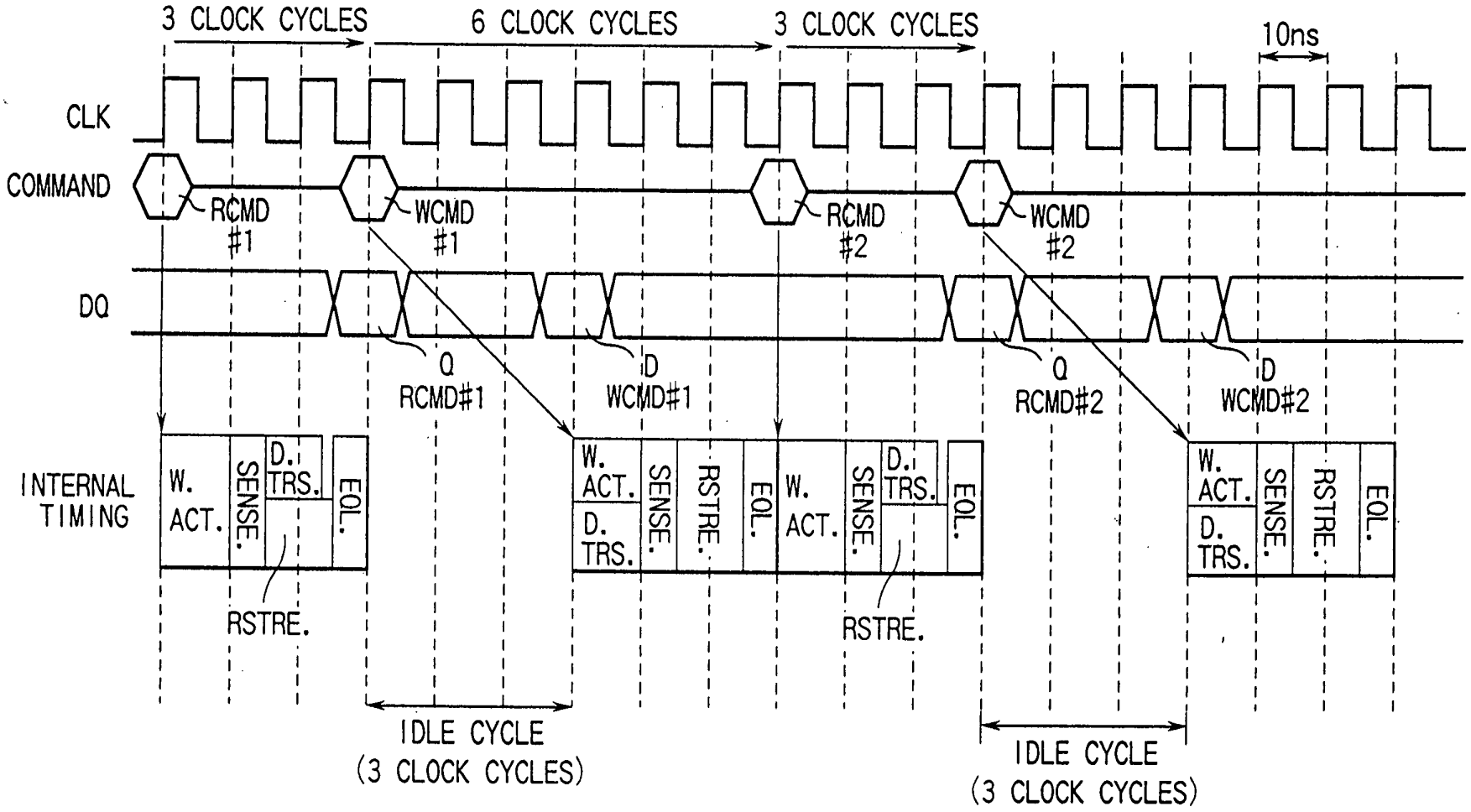
3 CLOCK CYCLES
6 CLOCK CYCLES
3 CLOCK CYCLES
10ns
CLK
COMMAND
RCMD #1
WCMD #1
RCMD #2
WCMD #2
DQ
Q RCMD#1
D WCMD#1
Q RCMD#2
D WCMD#2
INTERNAL TIMING
W. ACT.
SENSE.
D. TRS.
EQL.
RSTRE.
IDLE CYCLE (3 CLOCK CYCLES)
IDLE CYCLE (3 CLOCK CYCLES)

FIG. 9

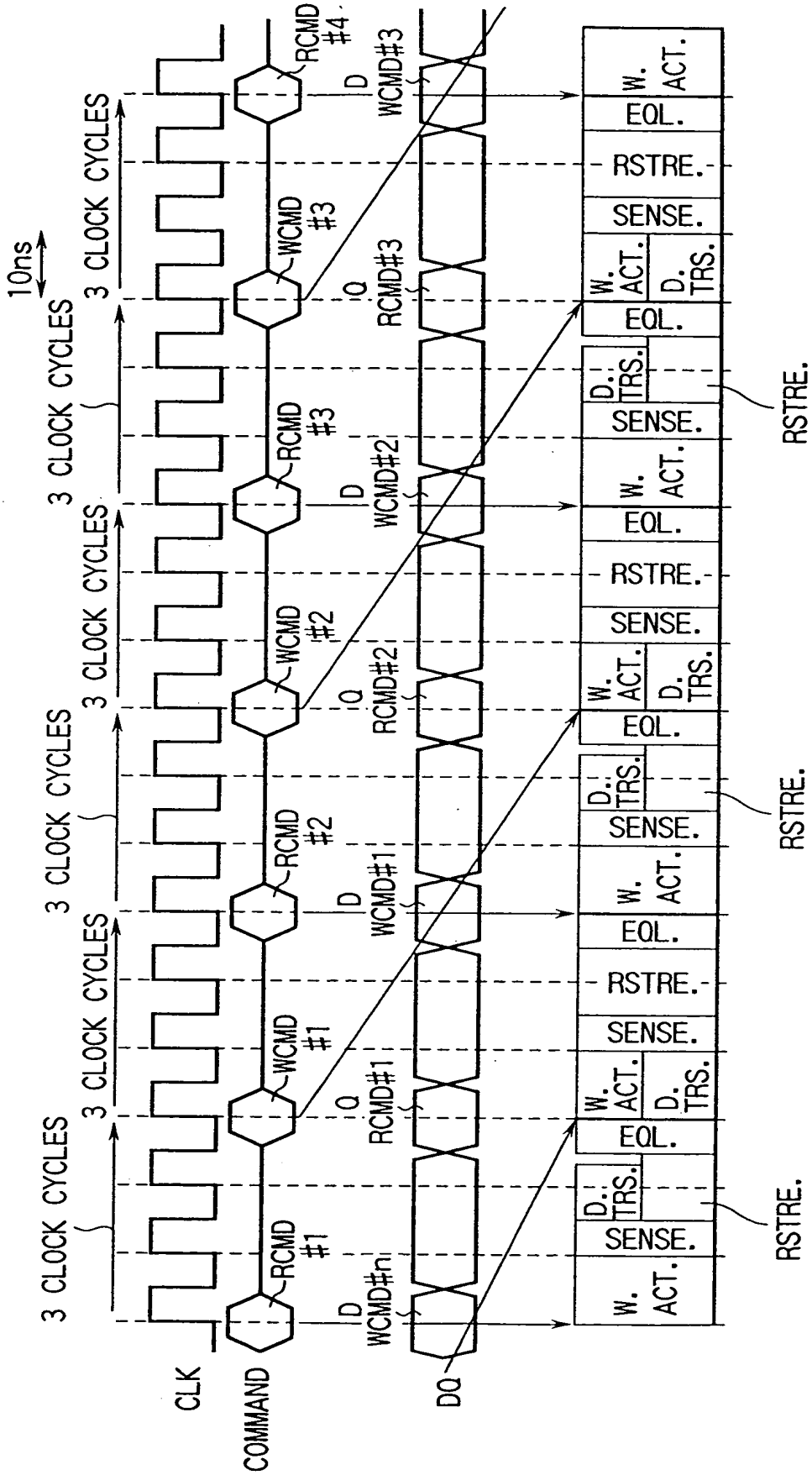
10ns
3 CLOCK CYCLES
CLK
COMMAND
DQ
RCMD #1
RCMD #2
RCMD #3
RCMD #4
WCMD #1
WCMD #2
WCMD #3
WCMD#n
D
Q
WCMD#1
WCMD#2
WCMD#3
RCMD#1
RCMD#2
RCMD#3
W. ACT.
EQL.
RSTRE.
SENSE.
D. TRS.
RSTRE.

FIG. 10

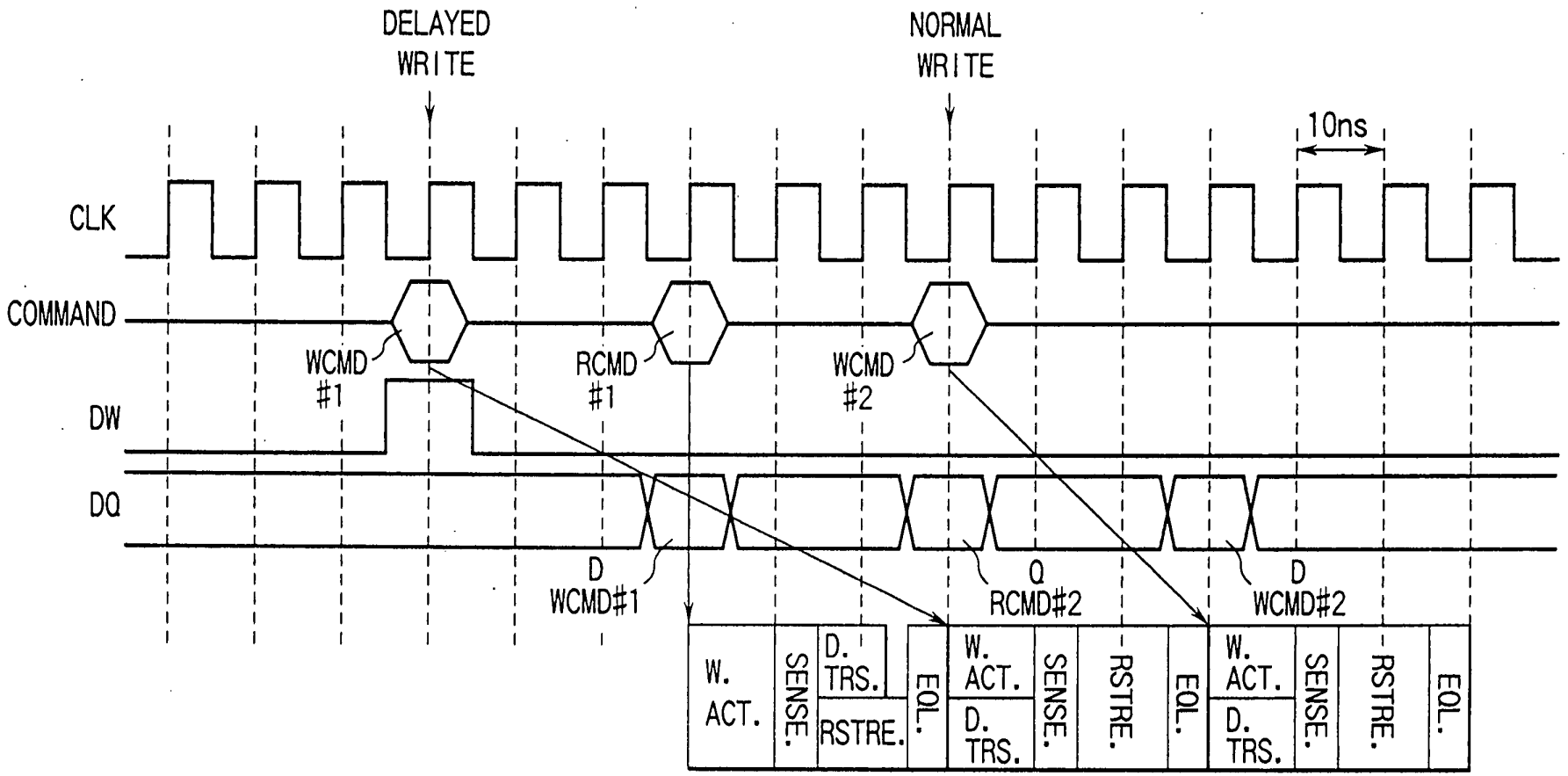
DELAYED
WRITE
NORMAL
WRITE
10ns
CLK
COMMAND
DW
DQ
WCMD
#1
RCMD
#1
WCMD
#2
D
WCMD#1
Q
RCMD#2
D
WCMD#2
W.
ACT.
SENSE.
D.
TRS.
RSTRE.
EQL.
W.
ACT.
D.
TRS.
SENSE.
RSTRE.
EQL.
W.
ACT.
D.
TRS.
SENSE.
RSTRE.
EQL.

FIG. 11

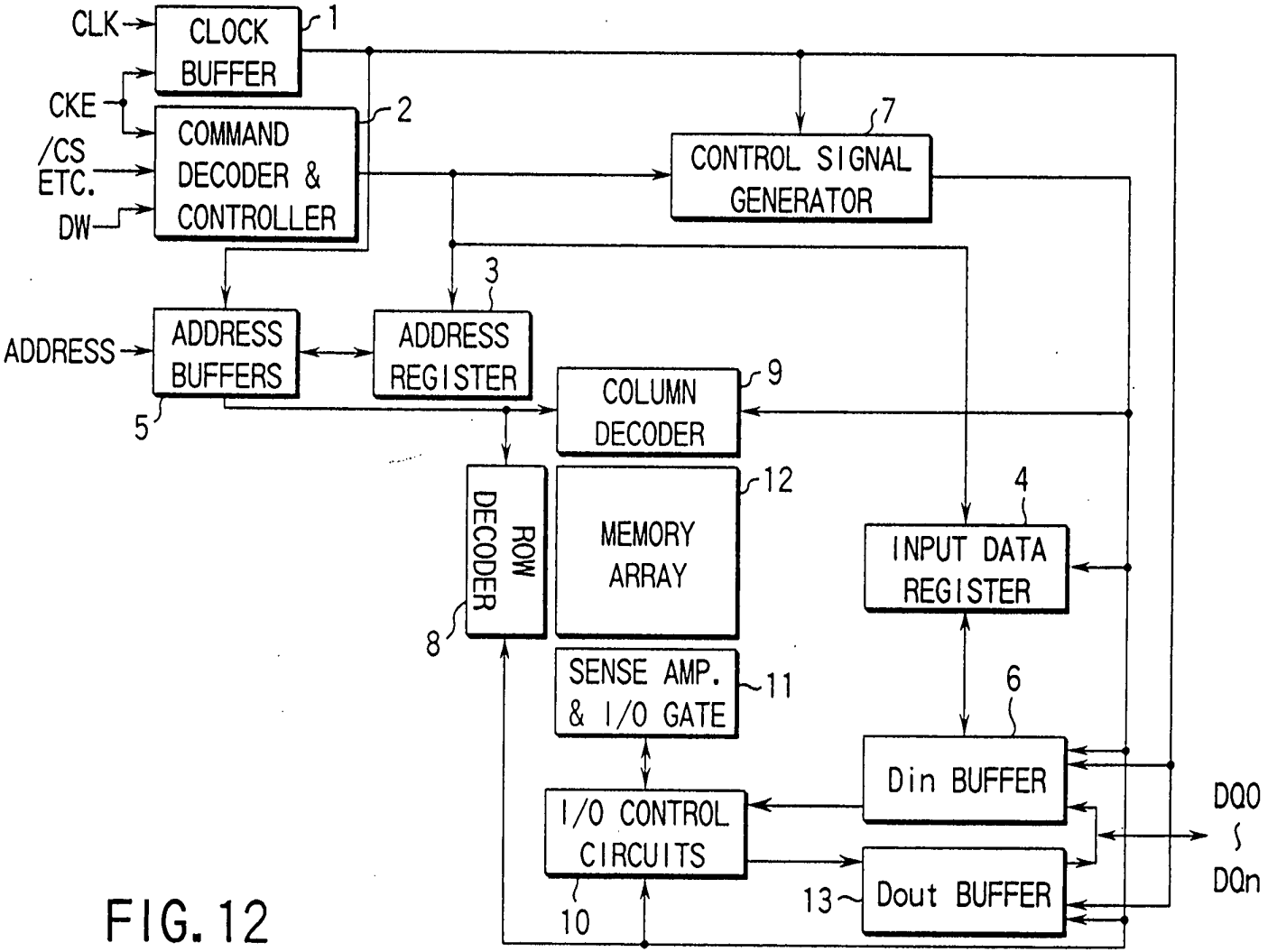
CLK
CLOCK BUFFER
1
CKE
/CS
ETC.
DW
COMMAND DECODER & CONTROLLER
2
CONTROL SIGNAL GENERATOR
7
3
ADDRESS
ADDRESS BUFFERS
ADDRESS REGISTER
5
COLUMN DECODER
9
ROW DECODER
8
MEMORY ARRAY
12
4
INPUT DATA REGISTER
SENSE AMP. & I/O GATE
11
6
Din BUFFER
I/O CONTROL CIRCUITS
10
13
Dout BUFFER
DQ0
~
DQn

FIG. 12

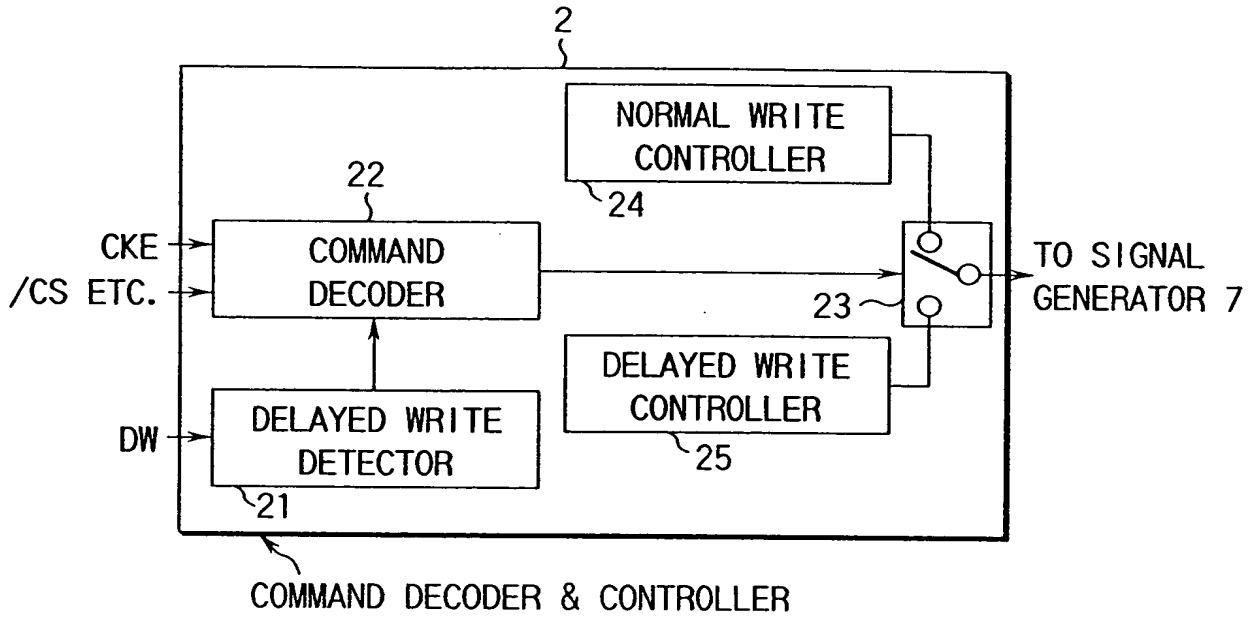

FIG. 13A

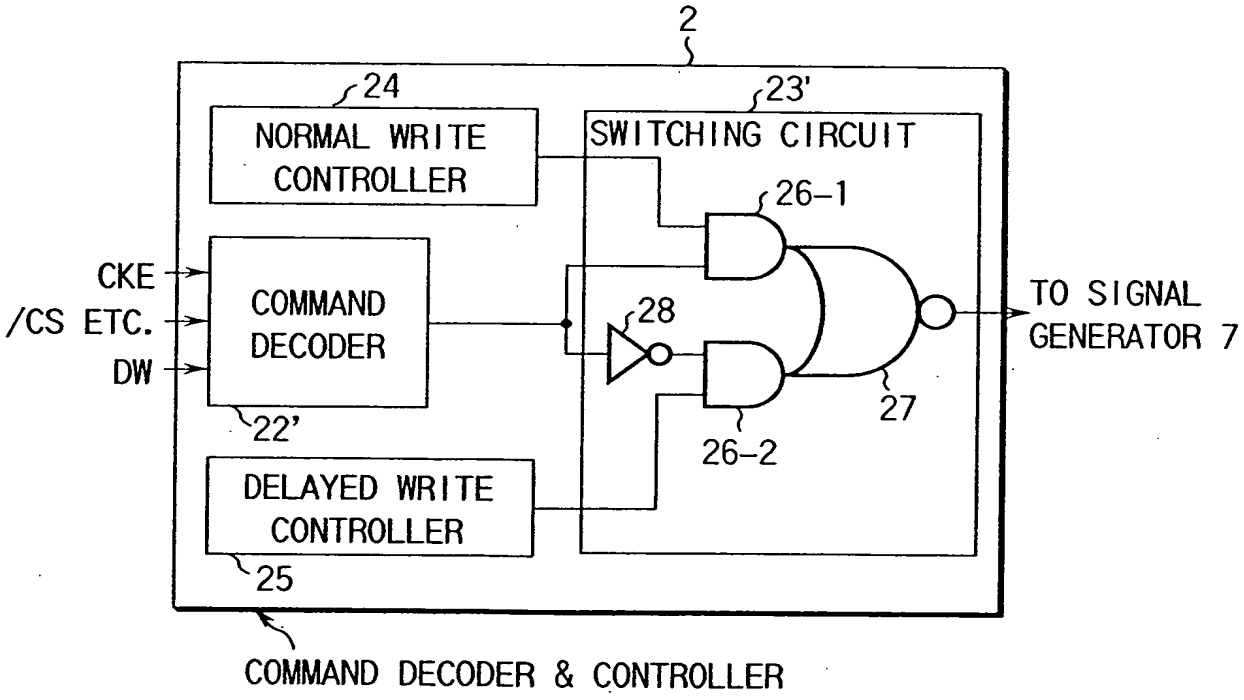

FIG. 13B

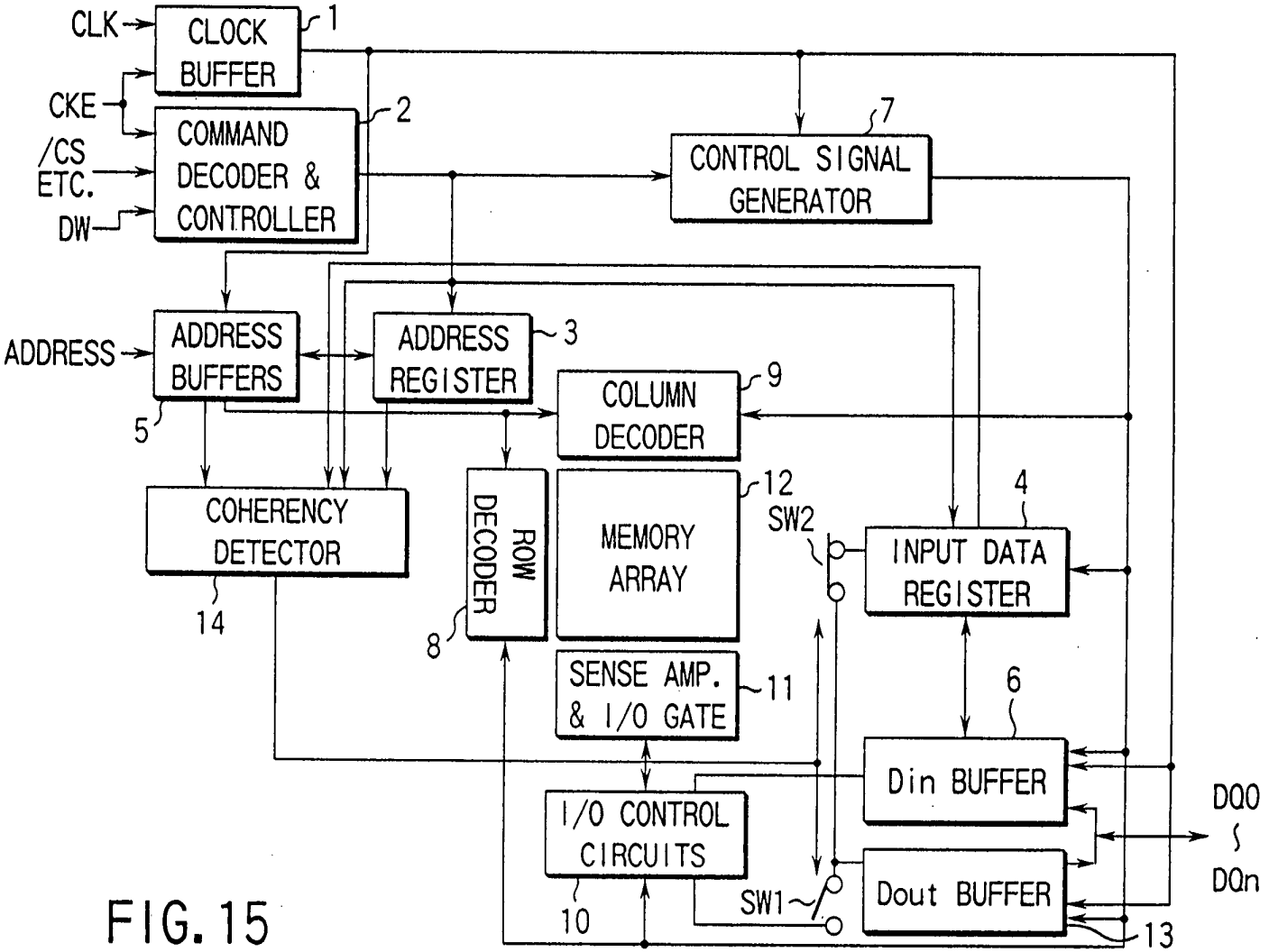
CLK
CLOCK BUFFER
1
CKE
/CS
ETC.
DW
COMMAND DECODER & CONTROLLER
2
CONTROL SIGNAL GENERATOR
7
ADDRESS
ADDRESS BUFFERS
5
ADDRESS REGISTER
3
COLUMN DECODER
9
COHERENCY DETECTOR
14
ROW DECODER
8
MEMORY ARRAY
12
SW2
4
INPUT DATA REGISTER
SENSE AMP. & I/O GATE
11
6
Din BUFFER
I/O CONTROL CIRCUITS
10
SW1
Dout BUFFER
13
DQ0
DQn

FIG. 15

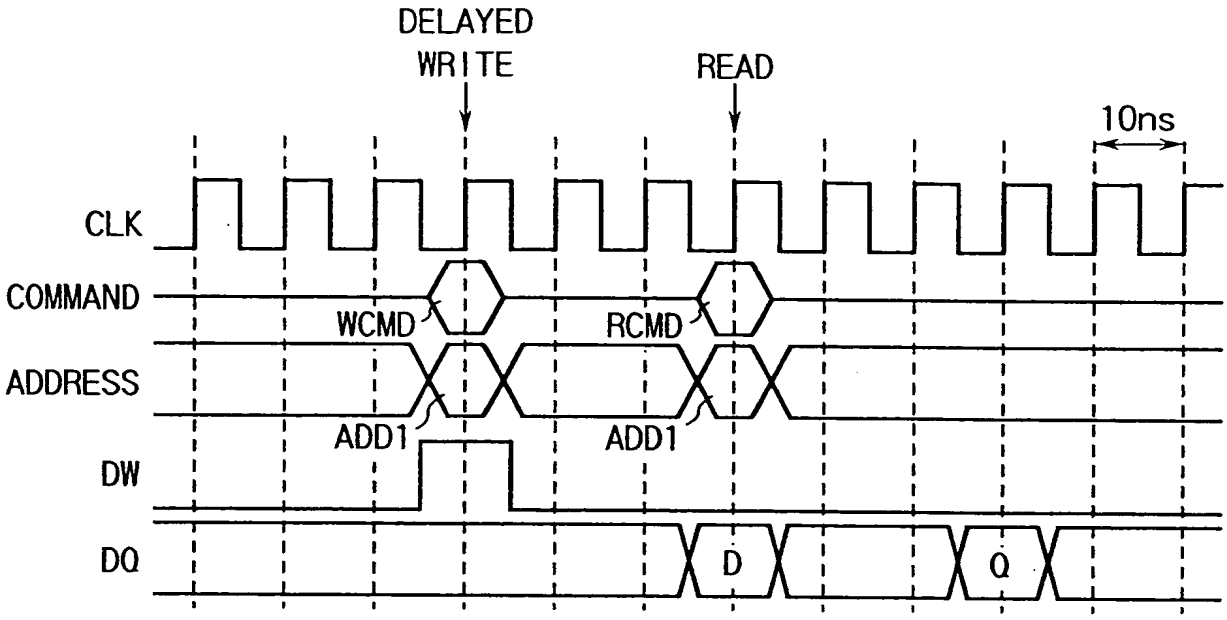

FIG. 14

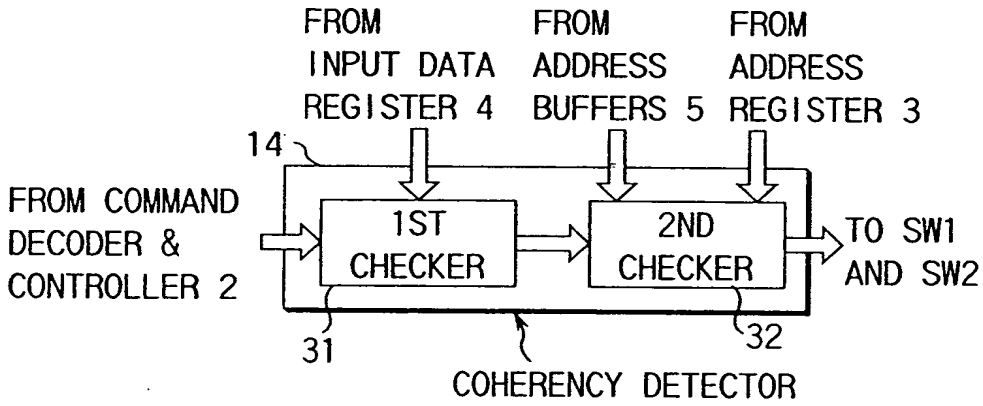

FIG. 16A

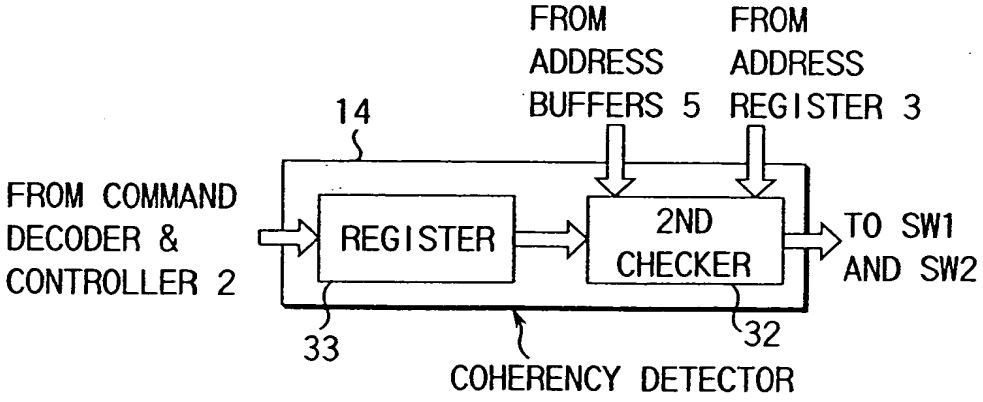

FIG. 16B

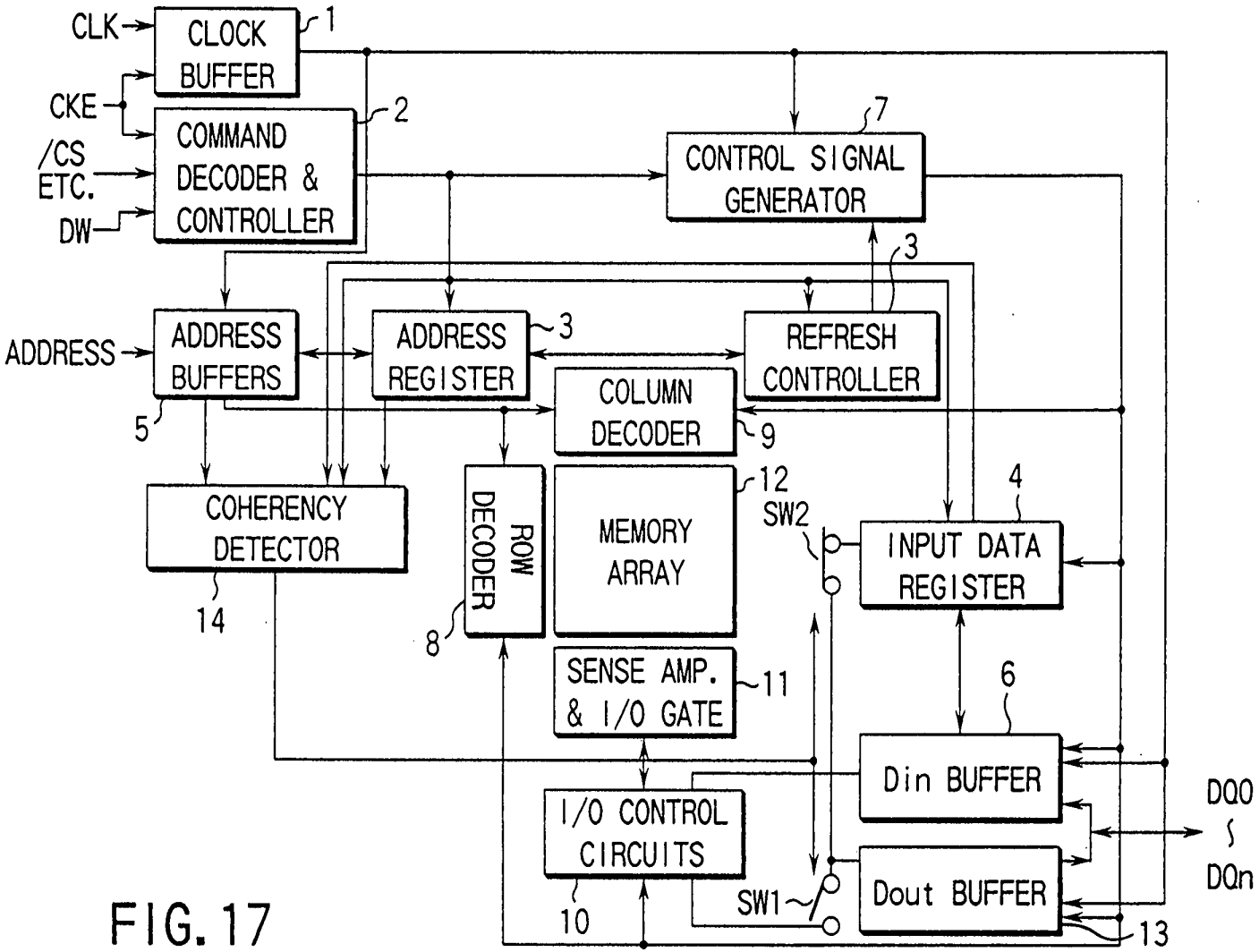
CLK
CLOCK BUFFER
1
CKE
/CS
ETC.
DW
COMMAND DECODER & CONTROLLER
2
CONTROL SIGNAL GENERATOR
7
3
ADDRESS
ADDRESS BUFFERS
5
ADDRESS REGISTER
3
REFRESH CONTROLLER
COLUMN DECODER
9
COHERENCY DETECTOR
14
ROW DECODER
8
MEMORY ARRAY
12
SW2
4
INPUT DATA REGISTER
SENSE AMP. & I/O GATE
11
6
Din BUFFER
I/O CONTROL CIRCUITS
10
SW1
Dout BUFFER
13
DQ0
DQn

FIG. 17

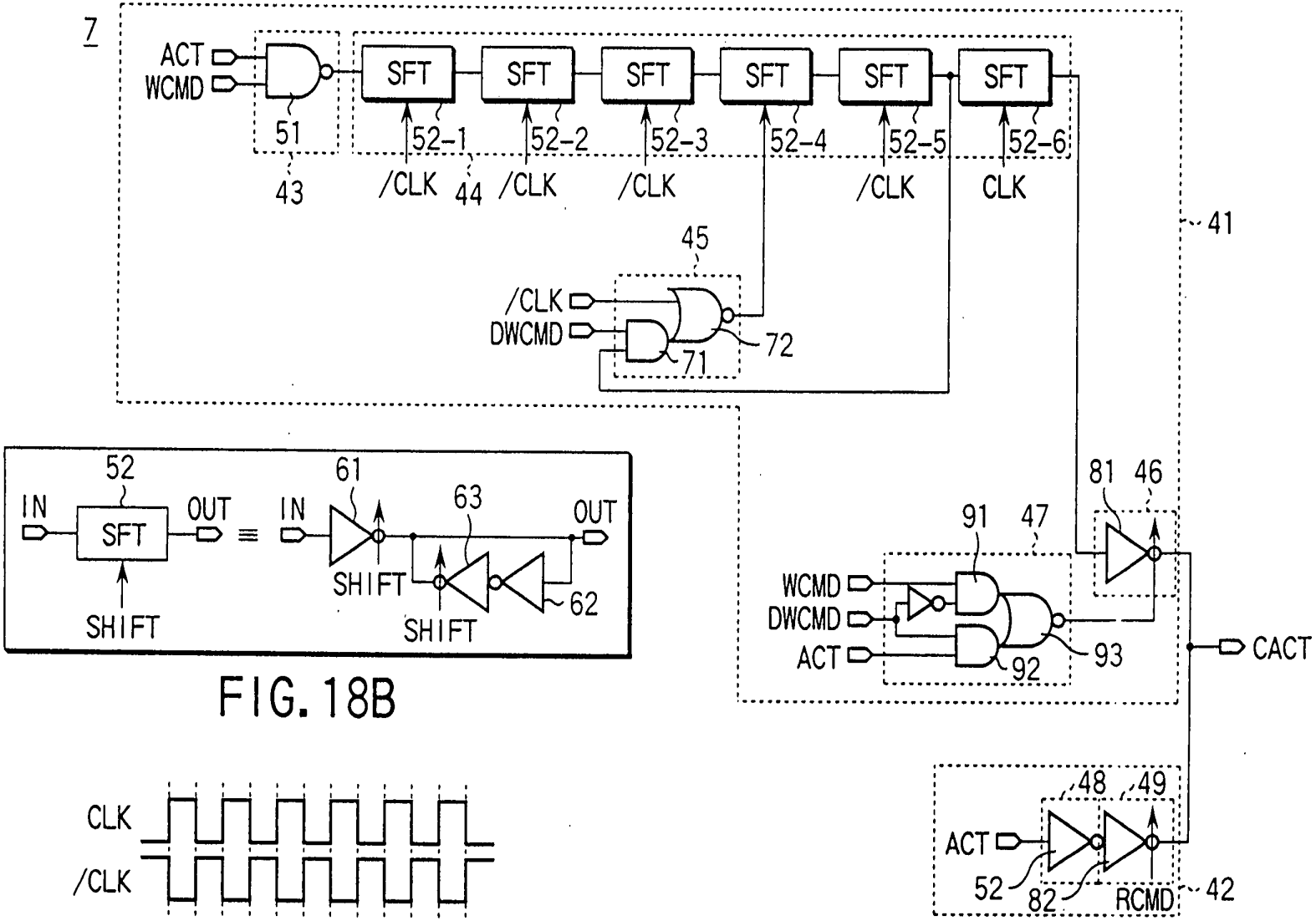

FIG. 18A

FIG. 18B

FIG. 18C

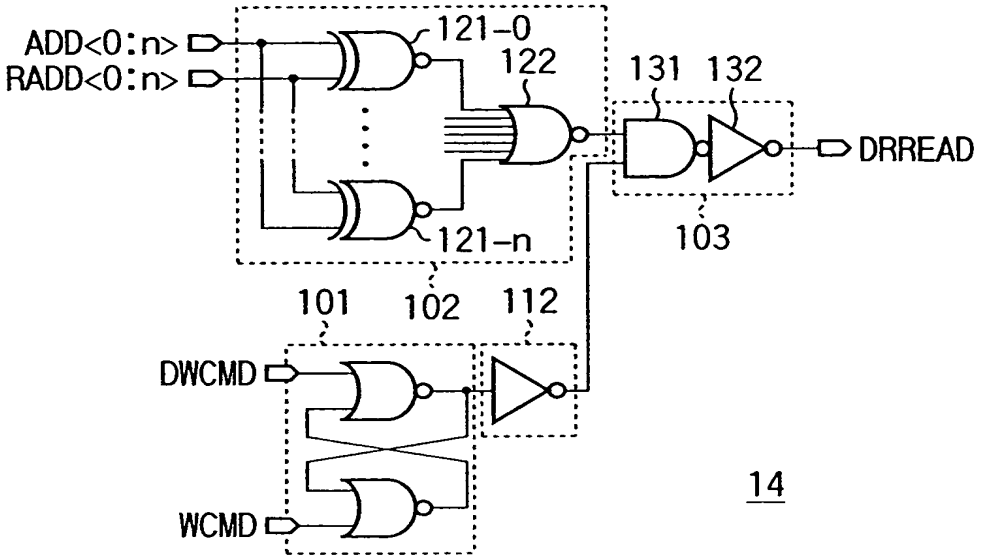
ADD<0:n>
RADD<0:n>
121-0
122
121-n
131
132
DRREAD
103
101
102
112
DWCMD
WCMD
14

FIG. 19

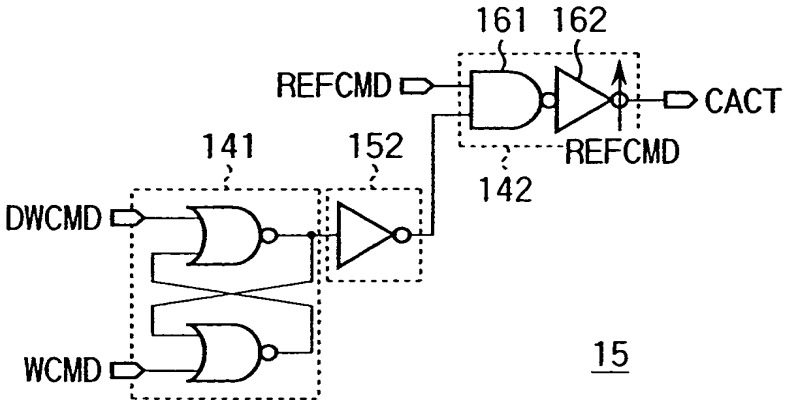
161
162
REFCMD
CACT
REFCMD
142
141
152
DWCMD
WCMD
15

FIG. 20